

# SwiShmem: Distributed Shared State Abstractions for Programmable Switches

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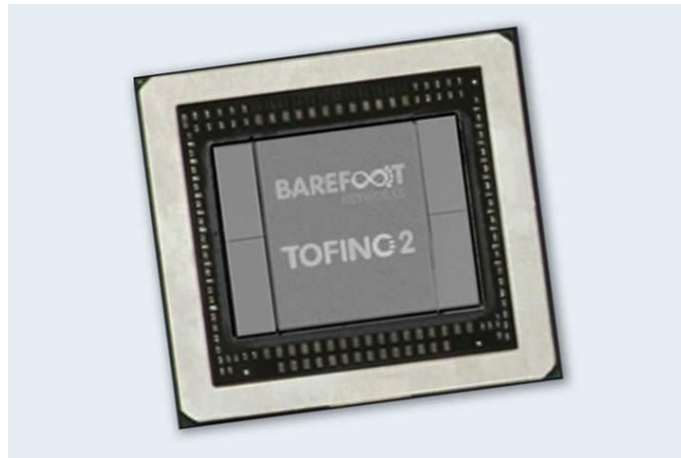
**Technion**  
Israel Institute  
of Technology



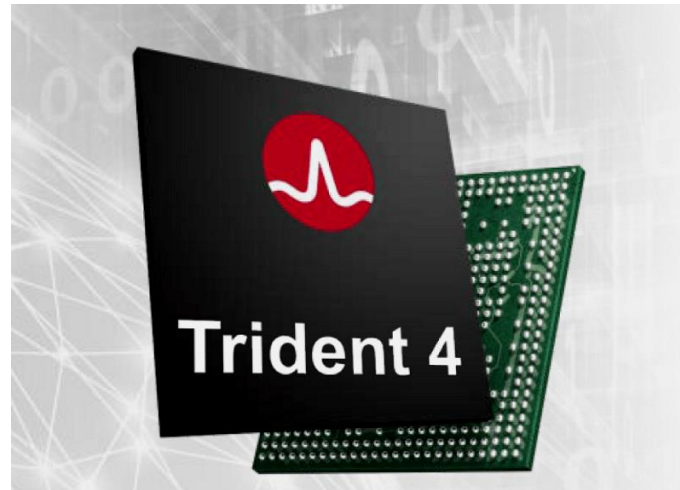
**Microsoft**

# Hardware Trend: PISA

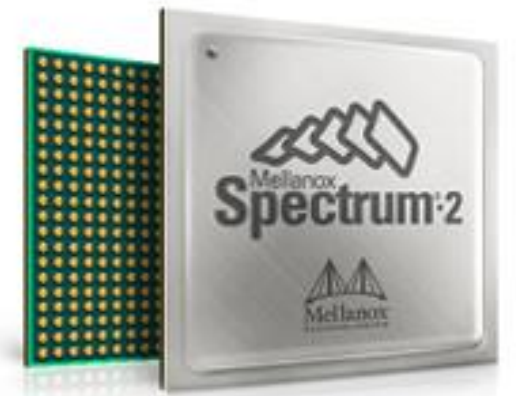
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**Barefoot Tofino**



**Broadcom Trident**



**NVIDIA Networking  
Spectrum**

# Current Trend: In-Switch Acceleration

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**SilkRoad: Making Stateful Layer-4 Load Balancing Fast and Cheap Using Switching ASICs**  
[SIGCOMM 2017]

**Offloading Real-time DDoS Attack Detection to Programmable Data Planes**  
[IM 2019]

**Heavy-Hitter Detection Entirely in the Data Plane**  
[SOSR 2017]

**Cheetah: Accelerating Database Queries with Switch Pruning**  
[SIGMOD 2020]

**Just say NO to Paxos Overhead: Replacing Consensus with Network Ordering**  
[OSDI 2016]

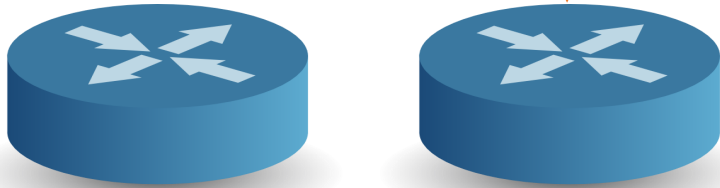
**NetCache: Balancing Key-Value Stores with Fast In-Network Caching**  
[SOSP 2017]



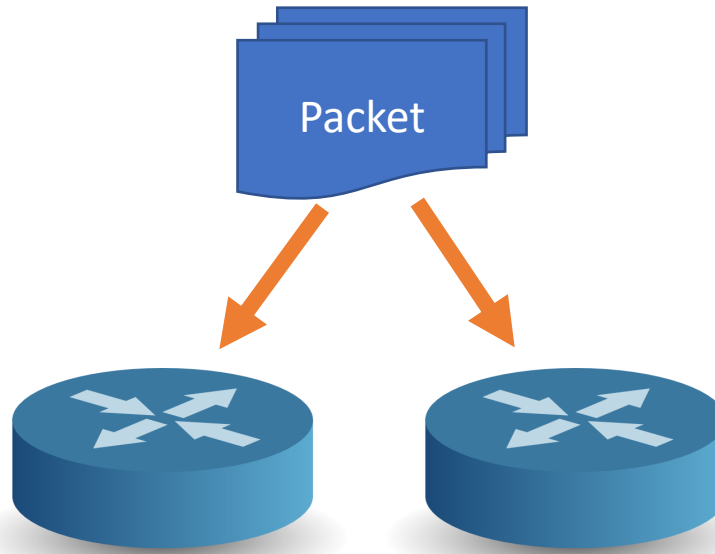
# Unrealized Potential

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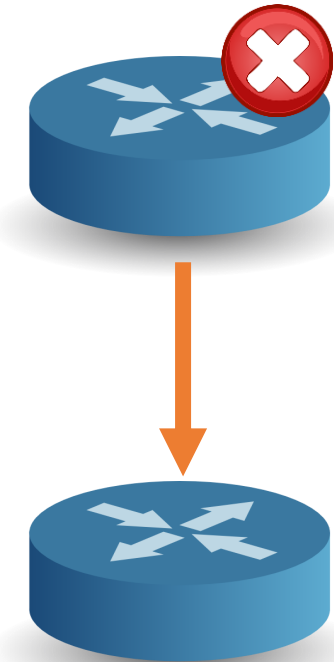
Scalability



Locality



Availability



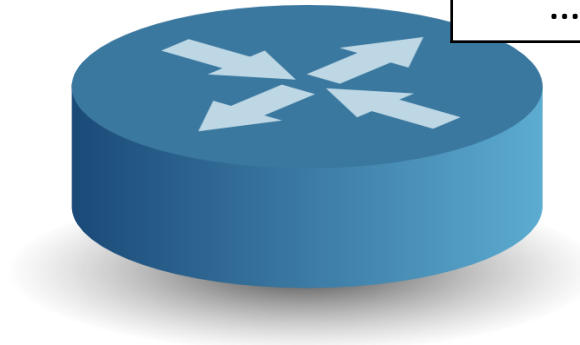
**Problem: Stateful + Distributed is a challenging combination**

# Network-Wide Heavy-Hitters Detection

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Data-plane updateable registers

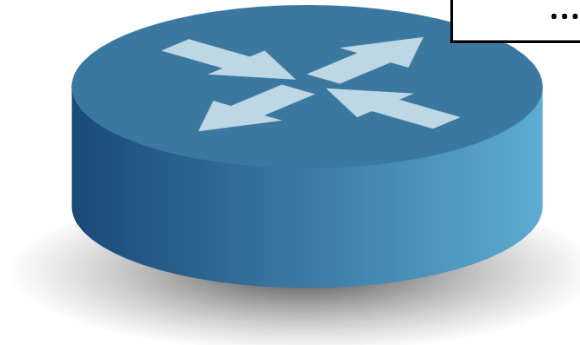
Match	Counter
flow <sub>0</sub>	128
flow <sub>1</sub>	64
flow <sub>2</sub>	1024
...	...



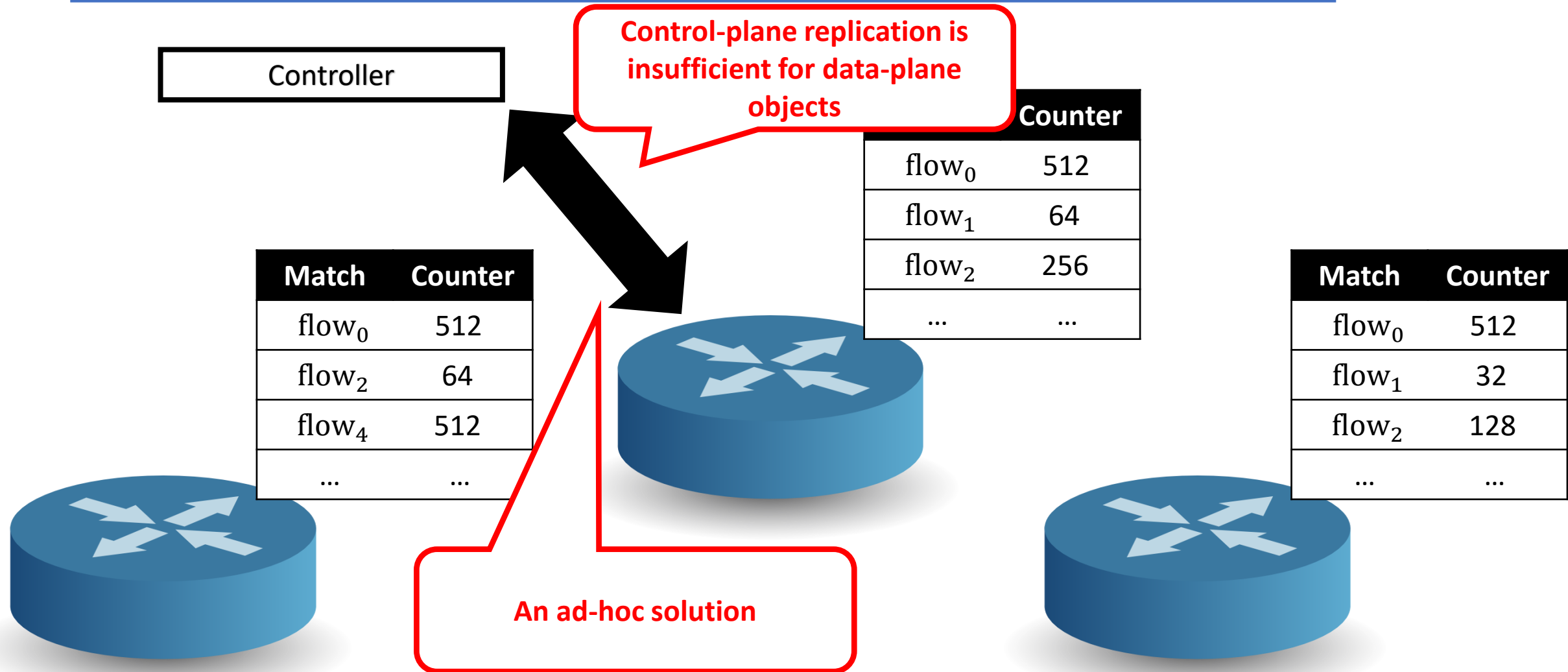
# Network-Wide Heavy-Hitters Detection

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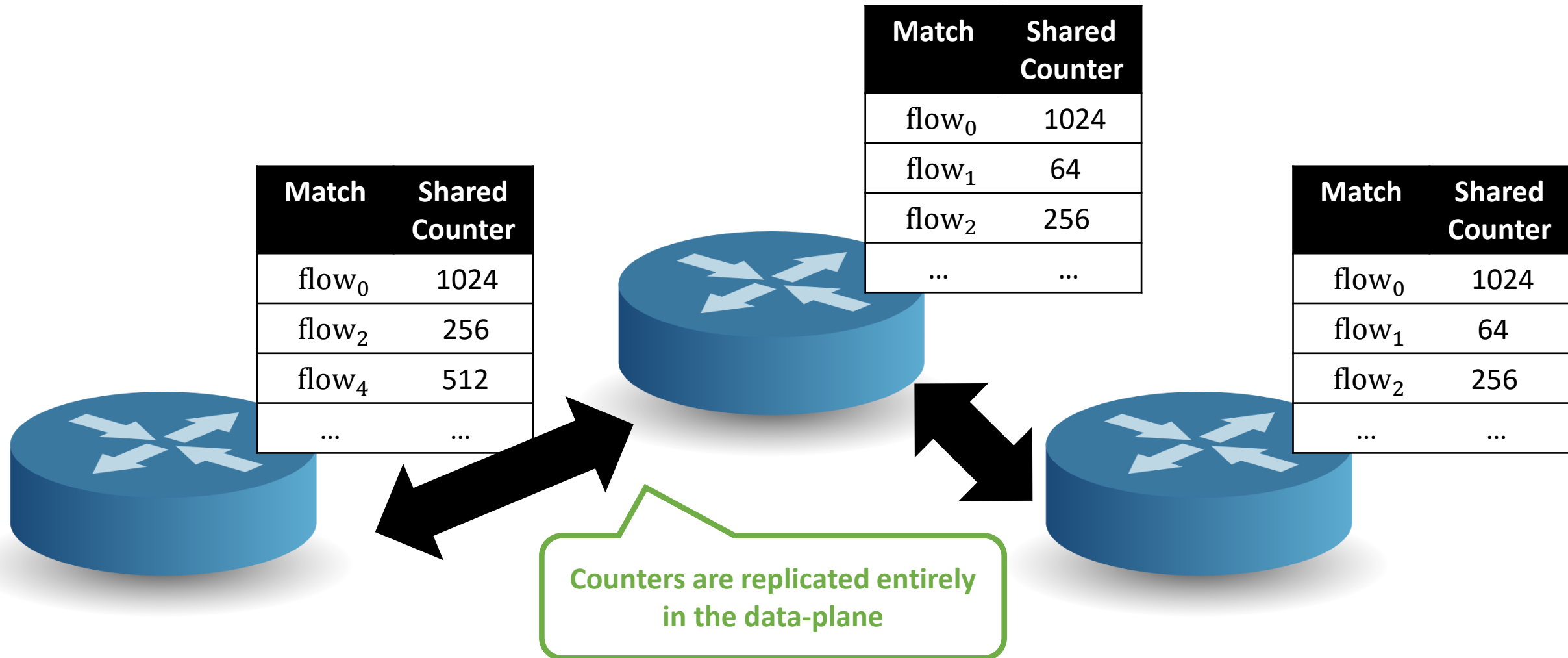
Match	Counter
flow <sub>0</sub>	128
flow <sub>1</sub>	64
flow <sub>2</sub>	1024
...	...



# Network-Wide Heavy-Hitters Detection



# Network-Wide Heavy-Hitters Detection





# A Principled Approach

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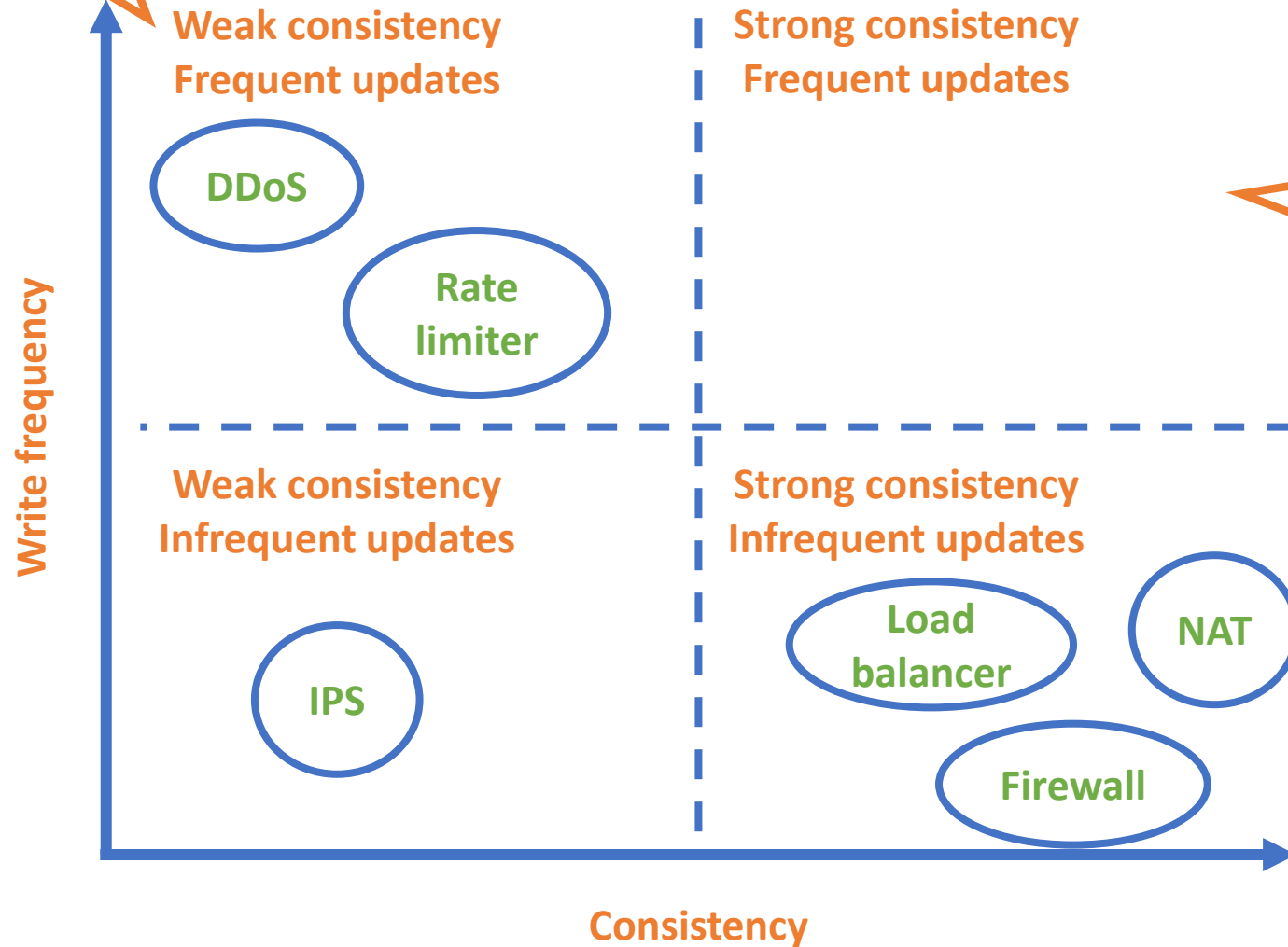
**Do not reinvent the wheel**



**Map proven and tested  
replication protocols**

Applications with frequent updates can tolerate weak consistency

# State Access in NFs



This combination is challenging

Strong consistency is often paired with infrequent updates

# SwiShmem Registers

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- Eventual Write-Optimized (EWO)
  - Eventual consistency (low read/write latency)
- Strong Read-Optimized (SRO)
  - Linearizability
- Eventual Read-Optimized (ERO)
  - Eventual consistency (lower read latency)

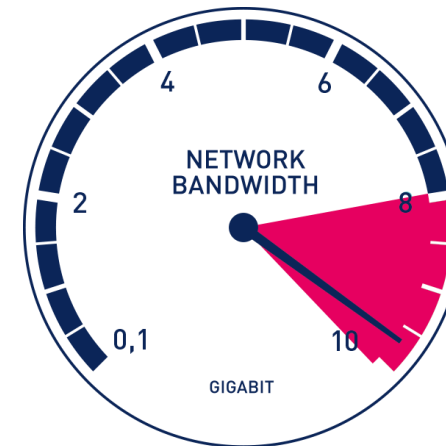
In the paper

# Design Principles

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**Memory is scarce ( $O(10\text{ MB})$  SRAM)**

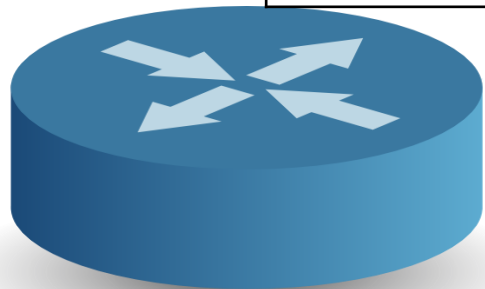


**Communication is cheap ( $O(5\text{ Tbps})$ )**

# Eventual Write-Optimized: HH Detection



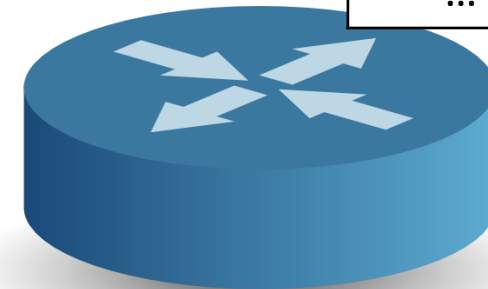
Match	Shared Counter
flow <sub>0</sub>	(0, 0, 0)
...	...



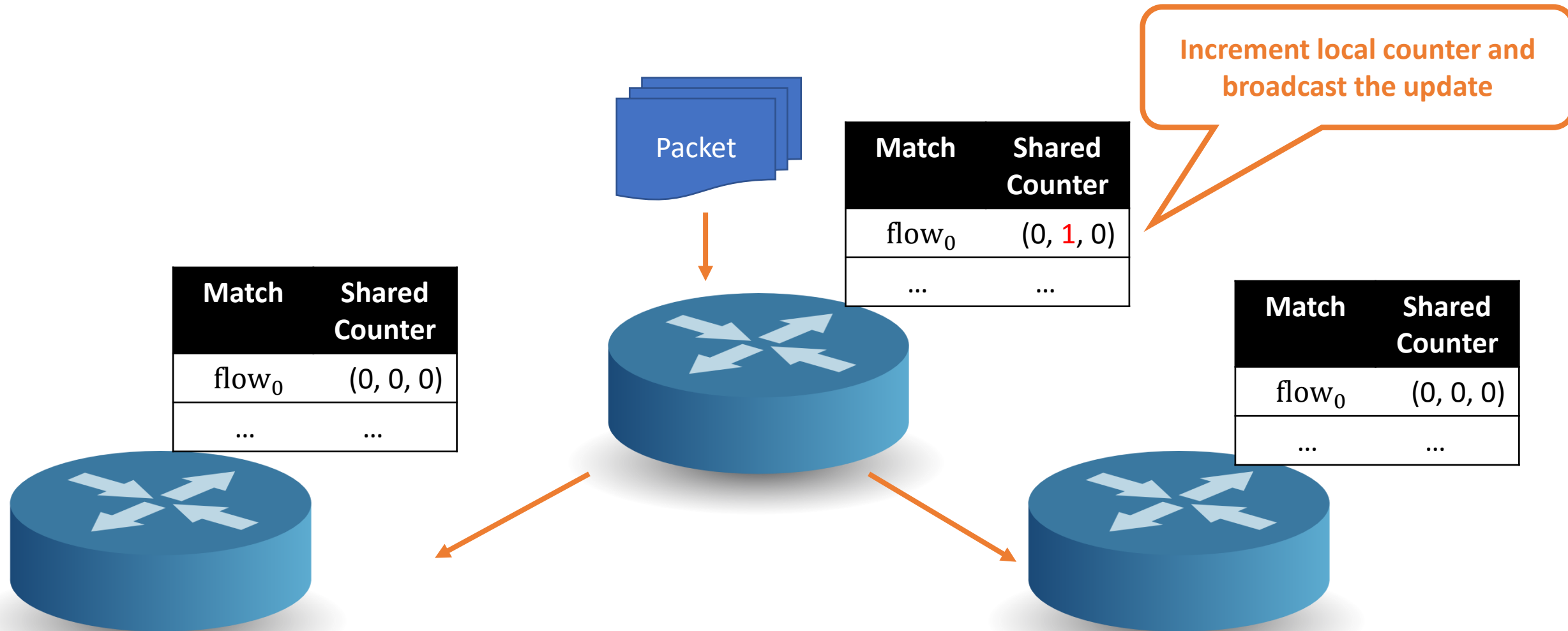
Match	Shared Counter
flow <sub>0</sub>	(0, 0, 0)
...	...



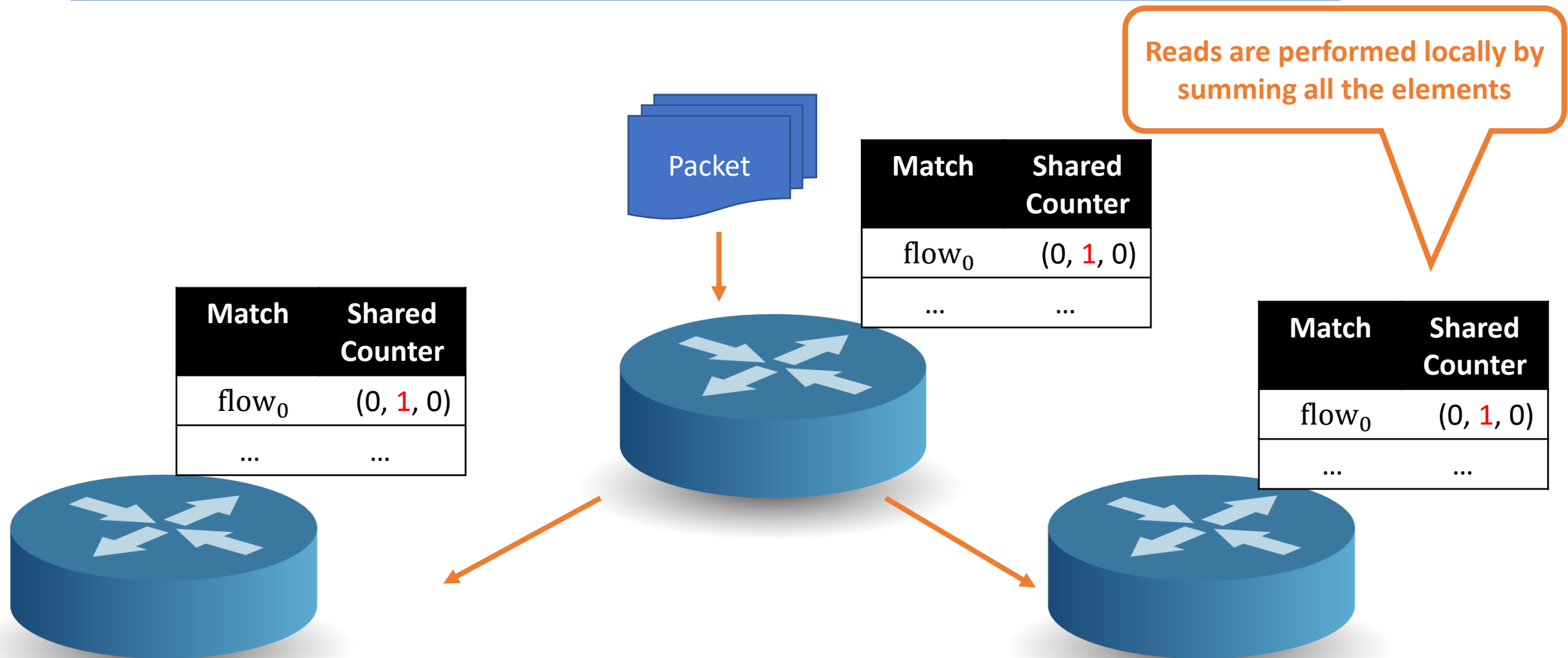
Match	Shared Counter
flow <sub>0</sub>	(0, 0, 0)
...	...



# Eventual Write-Optimized: HH Detection



# Eventual Write-Optimized: HH Detection



# What About Packet Loss?



Periodic synchronization

Match	Shared Counter
flow <sub>0</sub>	(0, 0, 0)
...	...

Match	Shared Counter
flow <sub>0</sub>	(0, 0, 0)
...	...

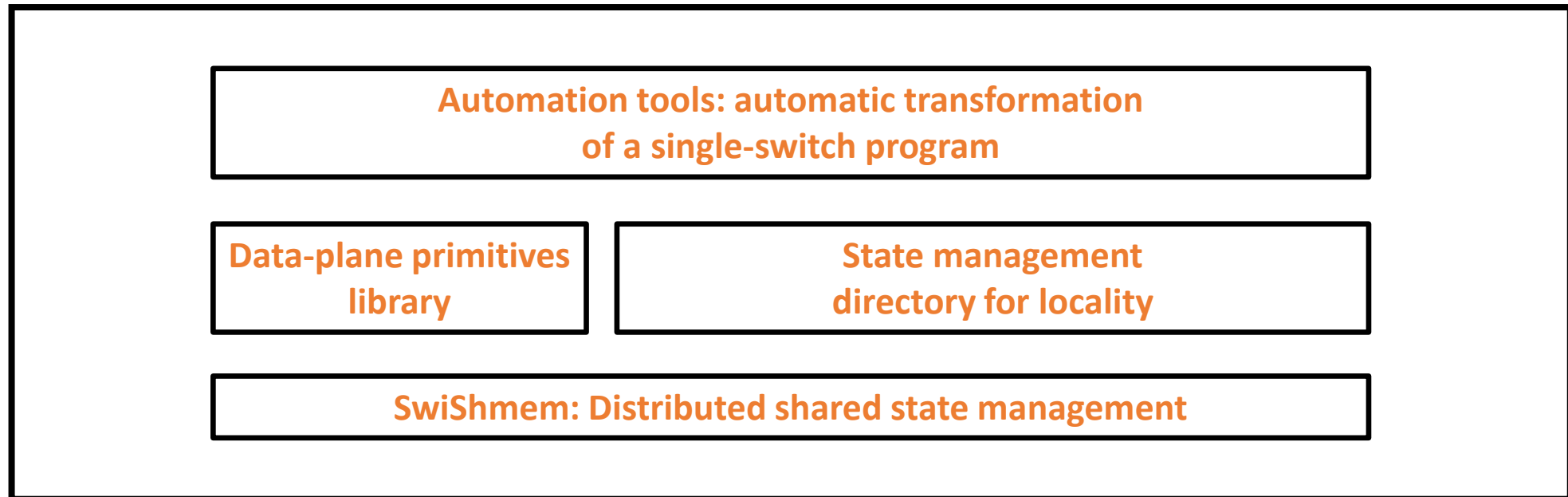
Match	Shared Counter
flow <sub>0</sub>	(0, 0, 0)
...	...

Updates may get lost



# Vision: “The One Big Switch Abstraction”

## The One Big Switch Abstraction



**Thank you!**  
**Questions?**